tion may be special service indicators, alpha-numeric messages, etc.

Graphically depicted in FIG. 2 are idealized intermittent ringing signals **201** and **202**, plotted with respect to time, with silent interval **203** therebetween. Commonly transmitted from a telephone central office on the ring lead of the station set, ringing signals such as **201** and **202** typically comprise a 20-hertz, 86-volt RMS sine-wave superimposed on −48 volts. Each ringing signal occurs for a time period of approximately two seconds followed by a silent interval such as **203** of approximately four seconds in duration. With a 20-hertz ringing signal, the time period of each ringing signal cycle is 50 milliseconds.

In accordance with this invention, a serial data message is sent during the first silent interval between intermittent ringing signals. A frequency shift keyed (FSK) signal such as **204** represents this data message and comprises two carrier frequencies sucn as 2025 and 2225 hertz which represent the low ("0") and high ("1") logic levels of the serial data message. The frequency shift keyed signal is received in a balanced manner on the tip and ring leads of the station set. This signal is transmitted from the central office by a data transmitter such as described in the copending application of this inventor, C. A. Doughty, Ser. No. 512955, filed concurrently on July 12, 1983, with this application, and entitled "Method and Apparatus for Sending a Data Message to a Selected Station during a Silent Interval between Ringing". Reference to this related application is made for a better understanding of the transmission of the data message during the silent interval between ringing. As shown, frequency shift keyed signal **204** is received a short time interval such as **205** after ringing signal **201**. This short time interval lasts, for example, 300 to 350 milliseconds to allow the station set to reach a steady state condition. During time interval **206**, a single frequency unmodulated FSK signal is received on the tip and ring leads of the station set to initialize the data receiver. During subsequent time interval **207**, a modulated FSK signal is received which represents the serial data message.

As shown in FIG. **1**, line interface unit **101** comprises high-pass filter **104**, difference amplifier **105** and band-pass filter **106**, which amplifies the modulated and unmodulated FSK signal and attenuates the 20-hertz ringing signals. High-pass filter **104** comprises blocking capacitors **107** and **108** which are serially connected to respective input leads **150** and **151** to block any DC voltage on the tip and ring leads of the station set. Also included are resistors **109** and **110** along with inductor **111** to attenuate any 20-hertz ringing signal which may be applied to difference amplifier **105**. Since the voltage level of the frequency shift keyed signal on the tip lead is equal in magnitude and opposite in polarity to the voltage level on the ring lead, difference amplifier **105** combines the two balanced input voltages to provide a single voltage input signal to band-pass filter **106**. Band-pass filter **106** passes the two carrier frequencies of the frequency shift keyed signal and greatly attenuates any other signals outside the frequency range of the two FSK signal frequencies.

Converter **102** converts the modulated FSK signal from the interface unit to a serial bit stream representative of the data message. In addition, converter **102** generates a carrier detect control signal indicating when a FSK signal is present. Converter **102** comprises well-known and commercially available frequency shift keyed modem **112** connected to a frequency standard such as crystal **113**. Only the demodulator portion of the modem is used to convert the modulated FSK signal to a serial bit stream. In addition, the modem generates the carrier detect control signal when a FSK signal is present.

The serial bit stream on output conductor **152** of converter **102** comprises a plurality of serial 8-bit characters each preceded by a start bit and followed by a stop bit. Depicted in FIG. **3** is the layout of a typical data message which comprises a plurality of 8-bit characters. The first 8-bit character **301** represents the message type such as a calling station directory number, an alpha-numeric message, special service indication, etc. The second character, character count **302** represents the number of subsequent data characters contained in the message followed by check sum **304**. Next, data characters **303** represent, for example, the digits of the calling station directory number, an alpha-numeric message, or any other indication which is intended to be displayed. When the data represents a directory number, each character represents two digits of the number beginning with the highest order digit of the number. Each digit is thus encoded as a 4-bit binary coded decimal character. The last character of the message, check sum character **304**, is the two's complement of the modulo **256** total of the character bytes of the message. Thus, when all the characters of the message are totaled, the sum should be zero if the message was received correctly.

The carrier detect control signal present on output conductor **153** of converter **102** assumes one of two logic levels when a FSK signal is present on input conductor **154** and assumes the other logic level when an FSK signal is not present.

Shown in FIG. **1**, control circuit **103** is the processing unit of on-hook data receiver **100**. Control circuit **103** performs two basic operations; namely, it interprets data messages received from converter **102** and sends special service information to alpha-numeric display **126**. Control circuit **103** comprises microprocessor **121**, program memory **122**, data memory **123**, address decoder **124**, UART **125**, and baud rate generator **127** which are all well-known and commercially available units. Also included are address bus **170** and data bus **171** which interconnect the various units as shown. Common to the various units of the control circuit are read (R) and write (W) conductors **157** and **158** for conveying read and write signals from microprocessor **121** to the other units of the control circuit. Individual select (S) conductors **172** through **176** from address decoder **124** are used to access program memory **122**, data memory **123**, UART **125**, and display **126**, respectively, in a well-known manner.

Microprocessor **121** is the information processing unit of the control circuit and executes the program instructions stored in program memory **121** to periodically update display **126**. Furthermore, responsive to the carrier detect control signal from converter **102**, microprocessor loads the characters of the data message into data memory **123**.

Program memory **122** is a permanent memory such as an erasable programmable read-only memory (EPROM) and stores program instructions which direct microprocessor **121** to sequentially perform its many functions.

Data memory **123** is a temporary and erasable memory such as a random access memory for storing infor-