mation related to the incoming message. The data memory comprises a message status block which is segmented to store a plurality of variables necessary to receive a data message. Depicted in FIG. **4** is the layout of the message status block (MSB) of the data memory which is segmented into a plurality of variables such as a MSB state, character count accumulator, check sum accumulator, input array pointer, and an output array pointer. Also included are larger segments of memory for an input and an output data array.

Universal asynchronous receiver transmitter (UART) **125** interfaces with microprocessor **121** to receive the serial data messages from converter **102**. These serial data messages are converted by UART **125** to a parallel format which are interpreted by microprocessor **121**. As previously mentioned, these serial format data messages include special service information such as the directory number of a calling station.

Responsive to address signals received on address bus **170** from microprocessor **121**, address decoder **124** selects program memory **122**, data memory **123**, UART **125**, and display **126** to receive address signals on address bus **170** and data signals on data bus **171**.

Baud rate generator **127** generates bit rate timing signals for UART **125**. For example, this timing signal has a bit rate of 16×300 baud which represents the baud rate of the incoming data message to UART **125**. Responsive to this timing signal on conductor **177**, UART **125** receives serial data characters on conductor **152**. Furthermore, UART **125** generates an interrupt signal to microprocessor **121** via conductor **178** when the carrier detect control signal on conductor **153** changes level or when a complete data character has been received.

Display unit **126** is a well-known and commercially available array of light-emitting diodes (LED's) or the like for displaying special service information from control circuit **103**. As suggested, this special service information may be the directory number of a calling station. Microprocessor **121** periodically updates each character of the display by selecting one of two well-known registers, a character address register and a data register of the unit (not shown), and writing data into these registers via data bus **171**. Selecting the character address register via select (S) conductor **175**, microprocessor **121** writes the address of the display character into the character address register via data bus **171** by activating write (W) conductor **158**. The contents of this register is then used to address the desired character in the display. In addition, selecting the data register via select (S) conductor **176**, microprocessor **121** writes the data register with the character for the desired display character location. Thus, each character of the display is periodically addressed to form a continuous display of the data message.

As previously mentioned, control circuit **103** performs two basic functions. The first is to interpret and store the data received in the receive buffer register of the UART, and the second is to periodically update the characters of the display with the stored data. These actions are accomplished by program instructions stored in the program memory which direct the microprocessor to perform the following functions: (1) recognize a start of message, (2) buffer data into data memory **123**, (3) check character count and check sum, (4) recognize loss of carrier, (5) recognize an excessive inter-character timing interval, (6) discard defective messages, and (7) unpack incoming BCD digits. The first basic operation involves receiving a data message from the central office for the associated called station. This data message includes special service information such as the directory number of the calling station in addition to a special service indicator. As previously described, the receipt of a data message is preceded by typically 90-milliseconds of a single frequency unmodulated FSK signal. This single frequency FSK signal causes converter **102** to send a carrier detect control signal to UART **125**. Responsive to the carrier detect control signal, UART **125** sends an interrupt signal to microprocessor **121**. This in turn causes microprocessor **121** to call an input interrupt routine which is stored in program memory **122**.

Depicted in FIG. **5** is the INPUT INTERRUPT routine which is called in response to an interrupt signal from UART **125**. The INPUT INTERRUPT routine is called in response to a plurality of events, thus making it necessary for the microprocessor to determine which event caused the interrupt. Microprocessor **121** determines the cause of the interrupt by reading a well-known status register (not shown) in the UART which contains the logic level of the carrier detect control signal. The bits of the status register are examined to determine whether the carrier detect control signal has changed logic levels or the UART receive buffer register has received a complete data character (block **501**). When the carrier detect control signal has changed logic levels to indicate the presence of a frequency shift keyed signal from the central office, a CARRIER DETECT routine is called (block **502**). When the status register indicates that a complete data character has been loaded in the UART receive buffer register, a CHARACTER READY routine is called (block **503**). When the INPUT INTERRUPT routine is completed, control is then returned to the base level program which is used to periodically update alpha-numeric display **126**.

Depicted in FIG. **6** is the CARRIER DETECT routine which is used to recognize the beginning of a data message. When an unmodulated single carrier frequency FSK signal has been detected (block **601**) microprocessor **121** sets the state of the message status block in data memory **123** to "type" (block **602**) and initializes the UART (block **603**). Microprocessor **121** initializes UART **125** by writing the status register of the UART. In response, UART **125** clears its receive buffer register in a well-known manner.

When the carrier detect control signal changes logic level to indicate the absence of a frequency shift keyed signal (block **601**), the state of the message status block is checked to determine whether it is "idle" (block **604**). When "idle", a complete data message has been received, as expected, and control is returned to the base level program. When the state of the message status block is not "idle", this indicates an abnormal termination of the data message transmission such as would happen when a customer lifts his receiver off hook during the transmission of a data message. As a result, the display is cleared (block **605**), and the message status block is set to "idle" (block **606**). Control is then returned to the INPUT INTERRUPT routine.

When the INPUT INTERRUPT routine indicates that a complete data character has been loaded in the UART receive buffer register, microprocessor **121** calls the CHARACTER READY routine which is depicted in FIG. **7**. The status register of the UART is then examined to determine whether the interrupt signal was